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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/695,853
Filing Date: October 28, 2003
Appellant(s): PAPPU ET AL.

Eric James Whitesell
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 4/4/2008 appealing from the Office action mailed 12/31/2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 5,828,579 | Beausang | 10-1998 |
| 6,457,161 | Nadeau-Dostie et al. | 9-2002 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

**Claims 1-20 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Beausang (5,828,579) in view of Nadeau-Dostie et al. (6,457,161).

**With respect to claims 1 and 10**, Beausang teaches a method of grouping cells for scan testing, which includes teaching a computer program/computer program product (description of CAD & computer system, Col 6, lines 1-42), comprising the steps of:

receiving as input a representation of an integrated circuit design (database [netlist] 210 that defines an IC design, acting as input to the system 205 of Figure 1B, Col 6, lines 53-55);

initializing (i.e. constructing) a corresponding list of cells for each of a plurality of common signal domains in the integrated circuit design (constructing scan chains [i.e. lists] being of a common clock domain, Col 4, lines 5-15), each corresponding list of cells created as an empty list (set of chains that are compatible with a particular clock domain may start out as empty, as suggested by 320 of Figure 2A);

selecting (i.e. accessing) a cell that belongs to one of the common signal domains and that is not included in a corresponding list of cells for any of the common signal domains (accessing segments [i.e. cell] that have not been assigned to a scan chain [list], Col 26, lines 60-65 & Col 27, lines 1-5); and

inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15).

Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver.

However, Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected (Col 7 line 67 to Col 8 line 57, i.e. signal tracing module).

It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

**With respect to claims 19 and 20**, Beausang teaches:

receiving as input a representation of an integrated circuit design (database [netlist] 210 that defines an IC design and acts as input data to the system 205 of Figure 1B, Col 6, lines 53-55) that includes cells (see clocked cells of Figures 6A-14B) clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains (see common signal domains of Figure 9A);

initializing (i.e. constructing) a corresponding list of cells for each of the common clock signal domains (constructing scan chains [i.e. lists] being of a common clock domain, Col 4, lines 5-15) by creating each corresponding list of cells as an empty list (set of chains that are compatible with a particular clock domain may start out as empty, as suggested by 320 of Figure 2A);

selecting (i.e. accessing) a cell having a clock signal input that is not included in a corresponding list of cells for any of the common clock signal domains (accessing segments [i.e. cell] that have not been assigned to a scan chain [list], Col 26, lines 60-65 & Col 27, lines 1-5);

inserting the selected cell in the corresponding list of cells for the common clock signal domain associated with the clock signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15);

Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver.

However, Nadeau-Dostie teaches: tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected to a common signal domain (Col 7 line 67 to Col 8 line 57, i.e. signal tracing module with the ability to trace signal inputs and identify their respective sources).

In addition, with respect to the recited "an integrated circuit design that includes cells clocked by a corresponding clock signal driver for one of a plurality of common clock signal domains", Nadeau-Dostie teaches said integrated circuit design with

common clock signal domains in Figure 7 (figure shows a common clock domain with drivers 74 and 84).

It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

**With respect to claims 2 and 11**, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 1 and 10, from which the respective claims depend, as described above. Beausang also teaches repeating steps (c), (d), (e), (f) and (g) until every cell belonging to the common signal domain associated with the signal driver has been inserted in a corresponding list of cells for the common signal domain, (accessing all segments [i.e. cells] that have not already been assigned to a scan chain and partitions the segments by clock domain).

**With respect to claims 3 and 12**, Beausang in view of Nadeau-Dostie et al. teaches all the elements of claims 2 and 11 respectively, from which the respective claims depend, as described above. Beausang also teaches generating as output a corresponding list of cells for a common signal domain in the integrated circuit design (generating as output a compiler generated script file which is a complete specification of the scan configuration, Col 10, lines 50-55, also see the figure in Col 10 indicating “scan chain 1” and “scan chain 2” and the cells they each contain).

**With respect to claims 4 and 13**, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10 respectively. Beausang teaches: wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver (during scan chain [i.e. list] construction, scan element name is included for each element, Col 16, lines 15-20, also see Col 10, lines 10-15).

**With respect to claims 5 and 14**, Beausang in view of Nadeau-Dostie teaches all the elements of claims 1 and 10, from which the respective claims depend, as discussed above. Beausang also teaches performing steps (b), (c), (d), (e), (f) and (g) for cells that are flip-flops in a scan chain (flip-flop is an example of a user defined segment, Col 14, lines 10-15).

**With respect to claims 6 and 15**, **Beausang** in view of **Nadeau-Dostie** teaches all the elements of claims 5 and 14, from which the claims depend respectively. **Beausang** teaches: performing steps (b), (c), (d), (f) and (g) for a common signal domain that is a scan clock domain (scan chains being of a common clock domain, Col 4, lines 1-15).

**With respect to claims 7 and 16**, Beausang in view of Nadeau-Dostie teaches all the elements of claims 6 and 15, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a net that is a clock net. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for a net that is a clock net (tracing backward from the clock input port of the latch to a clock

source, wherein the connection between the clock input port and the clock source is considered a “clock net”, Col 8, lines 1-15).

**With respect to claims 8 and 17**, Beausang in view of Nadeau-Dostie teaches all the elements of claims 7 and 16, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for an input port that is a clock port. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for an input port that is a clock port (clock input port of a latch, Col 8, lines 10-15).

**With respect to claims 9 and 18**, Beausang in view of Nadeau-Dostie teaches all the elements of claims 8 and 17, from which the claims depend respectively. Beausang does not teach: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver. However, Nadeau-Dostie teaches: performing steps (d), (e), (f) and (g) for a signal driver that is a clock driver (clock buffer 38 driven by a clock phase PH2 [i.e. driver], Col 4, lines 35-40).

**(10) Response to Argument**

**With respect to claims 1, 10, 19 and 20**: In page 7 of Appellant’s Appeal Brief, Appellant asserts: "because each and every step necessary to Beausang is presumed to be sufficiently disclosed under 35 USC S 112, the allegation that Beausang lacks sufficient disclosure for determining which scan chains have the same clock source is shown to be false. Examiner disagrees with this assertion.

Examiner points out that although Beausang provides sufficient disclosure for determining which scan chains have the same clock source (see Beausang, Col 27,

lines 24-30, “identified scan chains of that same clock domain”) Beausang fails to specifically describe a method step identical to the claimed method step "(d) tracing a net from an input port of the selected cell to a signal driver" and “(f) tracing the net to an input port of each cell connected to the signal driver”. Examiner points out that Beausang relies on the ability of one of ordinary skill in the art to determine which scan chains have the same clock source using one of many known methods in the art. One of these known methods is signal tracing in an electronic circuit design. Although Beausang fails to describe such a tracing process, Nadeau-Dostie teaches: "(d) tracing a net from an input port of the selected cell to a signal driver" (see Nadeau-Dostie, Col 8, lines 1-15, “tracing backward from the clock input [i.e. input port] of the latch to a clock source [i.e. signal driver]”) and “(f) tracing the net to an input port of each cell connected to the signal driver” (see Nadeau-Dostie, Col 8, lines 1-15, “tracing backward from the clock input [i.e. input port] of the latch to a clock source [i.e. signal driver]”).

**With respect to claims 1, 10, 19 and 20**: In page 7 of Appellant's Appeal Brief, Appellant asserts: "Because the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification of Beausang by Nadeau, the rejection of Claims 1, 10, 19 and 20 fails to support a prima facie conclusion of obviousness that would substantiate a rejection under 35 USC S 103". Examiner disagrees with this assertion.

Examiner points out “a reasonable suggestion for the desirability of making the proposed modification of Beausang by Nadeau” in page 2, numbered-section 5 of Examiner's FINAL office action mailed 12/31/2007, and it is as follows: It would have

been obvious to one with ordinary skill in the art at the time of the invention to incorporate the tracing steps of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide a clear explanation of one of several alternative methods for the identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang. Examiner relies upon Nadeau-Dostie to illustrate that such a tracing method, which helps to determine which scan cells/chains are connected to the same [i.e. any particular clock source] clock source, was well known in the art at the time of the invention.

**With respect to claims 1, 10, 19 and 20**: In page 8 of Appellant's Appeal Brief, Appellant asserts: "If the lacking step is not needed in Beausang to achieve its intended purpose as alleged by the rejection, then the motivating force for making the proposed modification of Beausang by Nadeau is based on the Applicant's disclosure, not on Beausang". Examiner disagrees with this assertion.

Examiner points out that the motivating force for making the proposed modification of Beausang by Nadeau-Dostie is based on the Beausang/Nadeau-Dostie combination and that of which is well known in the art at the time of the invention. The motivating force/suggestion is as follows: It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the tracing steps of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide a clear explanation of one of several

alternative methods for the identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain based of the method/system of Beausang. Examiner relies upon Nadeau-Dostie to illustrate that such a tracing method, which helps to determine which scan cells/chains are connected to the same [i.e. any particular clock source] clock source, was well known in the art at the time of the invention.

**With respect to claims 1, 10, 19 and 20:** In page 8 of Appellant's Appeal Brief, Appellant asserts: "If the lacking step is not needed in Beausang to achieve Beausang's intended purpose as alleged by the rejection, then the rejection fails to provide a reasonable suggestion for the desirability of making the proposed modification". Examiner disagrees with this assertion.

Examiner points out that the tracing step of Nadeau-Dostie is lacking in Beausang. However, the tracing step of Nadeau-Dostie is not "needed" to achieve Beausang's intended purpose; the tracing step of Nadeau-Dostie and the corresponding list of cells for a common signal domain of Beausang are two different inventions. Beausang relies upon the skills of one of ordinary skill in the art to use one of many acceptable alternative methods to determine which cells/chains correspond to which signal driver or clock driver(s). Nadeau-Dostie provides one acceptable method of making this determination by providing a method of signal tracing to determine which clock inputs correspond to which clock source(s).

**With respect to claims 1, 10, 19 and 20:** In page 9 of Appellant's Appeal Brief, Appellant asserts: "the rejection fails to disclose the last two steps recited in Claims 1, 10, 19 and 20 of tracing the net to an input port of the cell connected to the signal driver and inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver". Examiner disagrees with this assertion.

Examiner points out that the FINAL rejection mailed 12/31/2007 points out that the Beausang/Nadeau-Dostie combination clearly teaches the last two steps of claims 1, 10, 19 and 20. Beausang teaches: inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15).

Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver.

However, Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected (Col 7 line 67 to Col 8 line 57, i.e. signal tracing module).

It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into

the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

**With respect to claims 1, 10, 19 and 20:** In page 9 of Appellant's Appeal Brief, Appellant asserts: "The rejection fails to show that the proposed modification of Beausang by Nadeau-Dostie includes the steps recited in claims 1, 10, 19 and 20 of tracing the net to an input port of the cell connected to the signal driver and inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver". Examiner disagrees with this assertion.

Examiner points out that the FINAL rejection mailed 12/31/2007 points out that the Beausang/Nadeau-Dostie combination clearly teaches the last two steps of claims 1, 10, 19 and 20. Beausang teaches: inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver (scan segments inserted into scan chains wherein scan chains are of a common signal domain, Col 13, lines 55-60 & Col 4, lines 1-15).

Beausang does not specifically teach tracing steps that involve tracing a net to/from an input port of each cell connected to a signal driver.

However, Nadeau-Dostie et al. teaches a method/computer-tool for representing a circuit that involves tracing to/from an input port of each cell connected to a signal driver to identify the cells being connected (Col 7 line 67 to Col 8 line 57, i.e. signal tracing module).

It would have been obvious to one with ordinary skill in the art at the time of the invention to incorporate the teachings of Nadeau-Dostie et al. into the method/program of Beausang because the tracing step as taught by Nadeau-Dostie et al. would provide for the necessary identification of the scan cells for selection and further insertion into the lists (i.e. for proper partitioning of scan cells into subgroups) that correspond to a particular common signal domain of the method/system of Beausang.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be maintained.

June 19, 2008

Respectfully submitted,

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